REMARKS/ARGUMENTS

I. Introduction

Claims 1-13 and 19 are pending. Claims1, 4 and 10 have been amended.

In the Office Action the Examiner requested that Applicants resubmit a copy of the original information disclosure statement since the copy was missing from the file. **Applicants have complied with the Examiner's request and included a copy of the original information disclosure statement and references cited therein with this amendment.**

During a January 27, 2004 telephone interview the Examiner cited four additional patents (U.S. Patent Nos. 5,903,312; 5,815,206; and 5,870310 which were not originally cited in the Office Action. Applicants request that these references be listed in the next Office Action on an Examiner's list of cited references so that they will be of record in any patent that issues here from.

Applicants will summarize the telephone interview and address the rejections in detail below.

In view of the above amendment and the following remarks, it is respectfully submitted that the outstanding rejections have been overcome.

II. Interview Summary

This interview summary is presented in the format suggested by the Patent Office.

1. **Application Number: 09/442,363**
2. **Name of Applicant: Pearlstein et al.**
3. **Name of Examiner: Charles E. Parsons**
4. **Date of Interview: January 27, 2004**
5. **Type of Interview:** Telephonic
6. **Name of Participants:**
   Examiners: Charles E. Parsons, Andy Rao;
   Applicants' Rep: Michael P. Straub
7. **Exhibit(s) Shown:** None
8. **Claims discussed:** All the claims under consideration were discussed
9. **Prior Art Discussed:** The prior art applied in the Office Action was discussed. In particular Prior Art Fig. 1 found in the application and U.S. Patent No. 5,809,174 to Purcell et al. The Examiner also suggested that Applicants consider U.S. Patent Nos. 5,815,206; 5903312; and 5,870,310 but since copies of these patents were not before Applicants' representative they were not discussed in any detail during the interview.
10. **Proposed Amendments discussed:**

    No Amendments were proposed.

11. **Discussion of General Thrust of the Principal Arguments**

Applicants argued that the invention was directed to a novel use of a decoder circuit, e.g., hardware in combination with a programmable processor, e.g., a software controlled device, to perform image

decoding operations. In accordance with the invention the decoder circuit is used to perform non-memory intensive operations while the programmable processor is used to perform memory intensive operations.

Applicants argued that Fig. 1 of the application showed an all hardware decoder implementation. Accordingly, regardless of how the Examiner divided up the components any device or decoding method the Examiner would come up with based on Fig. 1 would still be entirely hardware (decoder circuit based) since Fig. 1 did not show a programmable processor or the use of a programmable processor. Accordingly, **it was argued that the rejection of Claim 1 and 19 under 35 USC. §103 was clearly not supported since Fig. 1 lacked a programmable processor. Since Fig. 1 lacks a programmable processor, to arrive at the claimed subject matter it is not merely a matter of "separating the function" of various components in Fig. 1, as asserted by the Examiner in the Office Action.** In view of these arguments Applicants requested that the rejection of claims 1 and 19 based on Fig. 1 of the Application be withdrawn.

With regard to the rejection of claims under 35 U.S.C. §103(a) based on Applicants Fig. 1 when considered in view of Purcell, **it was noted that the Examiner's stated position with regard to the teachings of the prior art actually would lead one away from implementing the decoding method as claimed and would definitely NOT result in the claimed combination.** The Examiner did not dispute that Fig. 1 illustrated a full hardware (circuit) implementation. In the Office Action the Examiner cited Purcell as teaching a decoder system where all processors

were programmable (see Office Action page 3 middle of the page). The Examiner proceeded to assert "…**it would have been obvious to one of ordinary skill in the art, to use dedicated processor for the memory intensive steps** in order to reduce the amount of time it takes to decode the image.) (Office Action page 4) Applicant's representative noted that they did not necessarily agree with the Examiner's interpretation of the art but that **if one of ordinary skill in the art was motivated to use a dedicated processor for the memory intensive steps as argued by the Examiner,** then one of ordinary skill in the art clearly would not end up with the claimed method which uses the **decoder circuit, e.g., "dedicated processor" to perform the non-memory intensive steps** and the programmable processor for the memory intensive steps as in the pending claims. Applicants noted that the claimed approach is somewhat unusual and, as discussed in the patent application, was based in part on bus considerations which are not discussed in the applied patent reference.

Applicants argued that it was clear that the proposed combination if made as the Examiner suggested, with dedicated hardware being used to perform memory intensive operations would not result in the claimed subject matter. For example, the combination would not result in the subject matter of claim 1 which recites:

> A method of decoding encoded image data comprising the steps of:
> **operating a decoder circuit implemented in hardware to perform at least one non-memory intensive image decoding operation** to generate, from the encoded image data, a first set of processed image

data, the at least one non-memory intensive image decoding operation being a variable length decoding operation;

supplying the first set of processed image data generated by the decoder circuit to a programmable processor; and

operating the programmable processor to perform at least one additional image decoding operation using the first set of processed image data.

The Examiner proceeded to argue that any and all combinations of Software/hardware decoding combinations were obvious. Applicants respectfully submitted that the Examiner had failed to cite any reference or prior art for this teaching and requested that the Examiner cite a reference or submit an affidavit setting forth the basis for this position if he intended to maintain the position so that Applicants could have a full and fair opportunity to respond. Applicants' strongly disagreed and noted that memory access and bus constraints played an important role in decoder design and that arguing that any and all possible combinations of splitting decoding functions between hardware and a programmable processor ignored and disregarded the problems of memory access, bus traffic and processing constraints, that one of ordinary skill in the art would normally consider in determining how to implement a decoder. Applicants representative noted that simply because a decoder implementation or decoding method that was NOT shown in the prior art could be implemented using existing elements or steps in a new combination did not in any way render the new combination obvious particularly where there was no teaching of the

combination or indication of a benefit of the combination in the art.

The Primary Examiner indicated that the existing rejections would probably be withdrawn but that new rejections could probably be made based on various references that he was aware of. The Examiner called back later and cited the 3 patents listed herein as references upon which a future rejection might be based. **Applicant's representative agreed to review the references and take them into consideration when filing a response to the outstanding office action.**

12. Other Pertinent Matters Discussed: None

13. General Results/Outcome of Interview

The Examiner indicated he would review Applicants formal written response to the Office Action upon its submission.

III. The Outstanding Rejections Have Been Overcome

In view of Applicant's arguments set forth in the interview summary, it is respectfully submitted that the rejections made in the Office Action should be withdrawn. Given that each of the rejections raised by the Examiner in the Office Action has been addressed, it is respectfully submitted that this amendment is fully responsive to the outstanding Office Action.

Should the Examiner seek to issue new rejections on additional references such as the 3 patents mentioned by

the Examiner during the interview, Applicants will address any such new rejections when they are formally presented.

IV. The Newly Cited References

Applicants representative is in the process of reviewing the newly cited references as suggested by the Examiner during the interview. However, given the brief amount of time between the date of the interview and the due date for the response, Applicants' representative has not had sufficient opportunity to consider the newly cited references in detail.

However, considering U.S. Patent No. 5,818,532 as being representative of the 3 cited patents, Applicants' representative notes the following:

A) from the abstract, the patent appears to **teach away from performing a variable length decoding operation using a dedicated circuit** as currently cited independent claims 1 and 4. In particular it is stated in the abstract "**MPEG-2 functions are performed by the hardware**: inverse can, inverse quantization, inverse discrete cosine transform, half pel compensation, and merge. **Other MPEG-2 functions such as** motion vector decoding, **variable length decoding,** and run level decoding **are not performed by hardware** …". (Bold added for emphasis)

B. Applicants did not see any indication in the patent that a **data reduction operation** is performed as part of the decoding operation. Accordingly, the patent

does not anticipate or render obvious claim 4 or 19 for this additional reason.

Applicants note that in the Office Action in regard to claims 3 and 4, the Examiner asserted:

> … wherein the step of operating the decoder circuit further includes: operating the decoder circuit to perform a data reduction operation. **(This is the purpose of decoders thus not a patentable element)**

Applicants respectfully disagree with the Examiner. The purpose of video decoders is to decode video data. Decoding of encoded (compressed) video or other data normally results **in an increase in the amount of video data** as compared to the encoded input. Accordingly, **data reduction is NOT the purpose of decoders as the Examiner asserts. If the Examiner seeks to maintain this position, Applicants respectfully request the Examiner cite support in a reference for this position.**

C. The Features of Claim 10 are Not Obvious or Anticipated

Claim 10 as amended recites:

The method of claim 8, further comprising the step of:

> storing in the decoder circuit **multiple sets of context information for different video streams** at the same time, **each set of stored context information corresponding to a different one of a plurality of encoded video data streams** processed by the decoder circuit each set of context information including vertical size, horizontal size and frame rate information.

The storing of multiple sets of context information of the type described allows the decoder circuit to be used to decode multiple bitstreams, e.g., in order to support picture-in-picture capabilities without the need for the information to be transmitted to the circuit each time a different one of the bitstream is to be decoded. (See Application page 19) This novel storage of multiple sets of context information is not disclosed in any of the applied references.

Applicants note that the different encoded data streams cited by the Examiner to reject claims 10, 11, 12 and 13 in the Purcell patent were not different video data streams but rather streams corresponding to different types of data, e.g., audio, video, etc. Applicants further note that the Examiner's reference to Purcell with regard to the decoder circuit is inconsistent with the Examiner's previous assertion that all the processors in Purcell were programmable. Applicants respectfully request that if the Examiner intends to rely on the Purcell reference he clarify what in Purcell he believes to correspond to a programmable processor and what, if anything, corresponds to the decoder circuit implemented in hardware that is recited in the claims.

V. Conclusion

In view of the foregoing amendments and remarks, the applicants respectfully submit that the pending claims are in condition for allowance. Accordingly, the applicants request that the Examiner pass this application to issue.

Applicants request that the Examiner contact Applicants' undersigned representative by phone if any outstanding issues remain to be resolved to place the application in condition for allowance.

Respectfully submitted,

February 6, 2004

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CERTIFICATE OF MAILING under 37 C.F.R. 1.8(a)

I hereby certify that this correspondence is being deposited on **February 6, 2004** with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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